11-21-00

A

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Marcus W. May et al.

Docket No. SIG000039

Title: METHOD AND APPARATUS FOR CONTROLLING POWER CONSUMPTION OF AN INTEGRATED CIRCUIT

Date: ~~11-14-2000~~ 11-20-00

To the Honorable Commissioner
of Patents and Trademarks
Box Patent Application
Washington, D.C. 20231

REQUEST FOR FILING A NATIONAL PATENT APPLICATION

The applicants respectfully request that the above captioned patent application be accepted for examination. This patent application is a:

[X] new patent application

[ ] continuation in part (CIP) of Application Serial No [ ] filed on [ ]

[ ] divisional application of Application Serial No. [ ] filed on [ ]

[ ] continuation application of Application Serial No. [ ] filed on [ ]

Accompanying this request is (as indicated by an "X" in the corresponding box).

[X] 1. 19 pages of specification, which includes the claims and abstract, and 5 sheets of formal drawings;

[X] 2. Combined Declaration and Power of Attorney;

[ ] 3. An Information Disclosure Statement along with the references;

[ ] 4. A petition to extend the response for a priority application identified above;

[X] 5. An assignment assigning all rights in the above referenced patent application to SigmaTel, Inc.;

[X] 6. An assignment recording cover sheet;

[X] 7. A verified statement establishing small entity status under 37 C.F.R. Sections 1.9 and 1.27;

[X] 8. A certificate of mailing indicating that the above captioned patent application has been deposited as "Express Mail" with the United States Postal Service;

[ ] 9. A certificate of mailing indicating that the above captioned patent application has been deposited with the United States Postal Service with sufficient postage as first class mail;

[X] 10. A return postcard; and

[ ] 11. A preliminary amendment.

The filing fee for the above captioned patent application is as follows:

Large entity status apply? no

				basic filing fee	355.00
total claims	22	extra per claim fee	9.00	extra claim fee	18.00
total ind claims	3	extra per ind claim fee	40.00	extra ind claim fee	0.00
				assign record fee	40.00
				TOTAL FILING FEE	413.00

Payment of the above calculated filing fee is as follows (as indicated by the "X" in the corresponding box):

[ ] A check in the amount of $

[X] Please charge Deposit Account No. 501415 in the amount of $ 413.00
A duplicate sheet is attached.

Respectfully submitted,

By: [signature]

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SIG000039

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Marcus W. May et al. Examiner:

Serial No. Art Group:

Filing Date: Docket No. SIG000039

Title: METHOD AND APPARATUS FOR CONTROLLING POWER CONSUMPTION OF AN INTEGRATED CIRCUIT

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11/20/00

To the Honorable Commissioner
of Patents and Trademarks
Washington, D.C 20231

STATEMENT OF STATUS AS SMALL ENTITY
Pursuant to 37 C.F.R. Section 1.27 and Section 1.9

For the above captioned patent application, a party in interest avers that it qualifies for small entity status as SMALL BUSINESS CONCERN. To verify the small entity status, the party in interest attests that:

1. This verified statement for the above captioned patent application or patent is being submitted prior to or with the first fee paid as a small entity;

2. For purposes of this verified statement, as defined in 37 C.F.R. Section 1.27, a license to a Federal agency resulting from a funding agreement with that agency pursuant to 35 U.S.C. 202 (c) (4) does not constitute a license.

3. As a SMALL BUSINESS CONCERN:
(a) I swear that I am an official of SigmaTel, Inc., empowered to act on behalf of SigmaTel, Inc.,
(b) In my capacity as identified in this section 3(a), I swear that SigmaTel, Inc. qualifies as a small business concern as defined in 37 C.F.R Section 1.9 and that the number of employees of SigmaTel, Inc. and those of its affiliates, does not exceed 500 persons;
(c) I further swear that my signature appears at the end of this Statement of Status as Small Entity,
(d) I still further swear that, in support my of contention that SigmaTel, Inc qualifies as a small business concern, exclusive rights to the invention of the above captioned patent application have been conveyed to and remain with SigmaTel, Inc.,

Signatures of Person(s) Making the Verified Statement

SigmaTel, Inc. (Customer No 000024263)
Name: Timothy W. Markison

Signature

Date 11/20/00

Title: General Counsel

PATENT APPLICATION

SIG000039

A METHOD AND APPARATUS FOR CONTROLLING POWER CONSUMPTION OF AN INTEGRATED CIRCUIT

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to integrated circuits and more particularly to controlling power consumption by an integrated circuit.

BACKGROUND OF THE INVENTION

Integrated circuits (IC's) are known to be used in a wide variety of electronic devices. For example, personal computers, cellular telephones, compact disk players, MP3 players, et cetera all include integrated circuits. Such integrated circuits are comprised of a plurality of functional circuit blocks that perform desired functions. Transistors, resistors and capacitors generally comprise the circuitry found in each circuit block.

As is known, transistor performance (e.g. transfer characteristics, on resistance, slew rate, et cetera) varies depending on the supply voltage. The lower the supply voltage, the lower the transistor performance and slew rate, but the less power it consumes. Conversely, the higher the supply voltage, the higher the performance and slew rate, but more power is consumed. As such, the power consumption by an integrated circuit is very much dependent on the supply voltage and transistors that comprise the circuit blocks.

As processing speeds of microprocessors, digital signal processors, et cetera increase, such devices are capable of processing larger software applications in less time. While some applications push the processing engine to its processing speed limits, most applications do not. However, the processing engine must be designed to support the highest processing requirements. Thus, the processing engine needs to have a supply voltage and system clock to handle the most taxing applications. When the processing engine is executing less taxing applications, the voltage and system clock remain the same, thus power consumption of the integrated circuit remains the same even though the application could accurately be performed with a lower supply voltage and/or a lower system clock.

Therefore, a need exists for a method and apparatus that adjust the system clock and/or the supply voltage based on the processing capabilities of an integrated circuit and the application being performed to conserve power.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a schematic block diagram of an integrated circuit in accordance with the present invention;

Figure 2 illustrates a schematic block diagram of an alternate integrated circuit in accordance with the present invention;

Figure 3 illustrates a schematic block diagram of a multiply accumulator in accordance with the present invention;

Figure 4 illustrates a graphical representation of adjusting the supply clock and/or the supply in accordance with the present invention;

Figure 5 illustrates a schematic block diagram of a power controlling apparatus in accordance with the present invention;

Figure 6 illustrates a logic diagram of a method for controlling power consumption of an integrated circuit in accordance with the present invention; and

Figure 7 illustrates a logic diagram of further processing of steps in Figure 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Generally, the present invention provides a method and apparatus for controlling power consumption of an integrated circuit. Such a method and apparatus include processing that begins by producing a system clock from a reference clock based on a system clock control signal. The reference clock may be generated from an external crystal oscillator circuit operable to produce a reference clock at a desired frequency. The processing continues by regulating at least one supply from a power source and an inductor based on a power supply control signal, or a linear regulator. The processing continues by producing the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computational engine and processing requirements associated with processing at least a portion of an application by the computational engine. With such a method and apparatus, power consumption of an integrated circuit can be controlled, and thereby reduced, based on the application being performed by the computational engine and the capabilities of the computational engine within the integrated circuit thereby reducing power consumption.

The present invention can be more fully described with reference to Figures 1 through 7. Figure 1 illustrates an integrated circuit 10 that includes a phase lock loop 16, a computational engine 12, memory 14 and an on-chip power supply 20. The integrated circuit 10 is operably coupled to an external inductor 60 and an external power source 62 (e.g. a battery). The computational engine 12 may be a microprocessor, coprocessor, digital signal processor, logic circuit, state machine, analog circuit, and/or any circuitry that manipulates signals (analog or digital) based on operational instructions. The memory 14 may be on-chip or off-chip and stores a power savings algorithm 22, and at

least one application. In this illustration the memory is storing two applications 24 and 26. As one of average skill in the art will appreciate, many more applications may be stored in memory 14 than the two illustrated.

The phase lock loop 16 is shown to include a 1st divider 28, a 1st register 29, a phase comparator 30, a charge pump 32, a voltage controlled oscillator 34, a 2nd divider 36, a 2nd register 37, a 3rd divider 38, and a 3rd register 39. In practice, the phase lock loop 16 may include one, two, or three of the dividers 28, 36 and 38 to produce the system clock 42 from the reference clock 40. The registers 29, 37 and 39 each store values to represent the corresponding divider value. For example, divider 28 utilizes one of the values in register 29 to produce a (÷ M) function. Similarly, divider 36 utilizes values in register 37 to produce a (÷ P) value and divider 38 utilizes values in register 39 to produce a (÷ N) value.

In operation, the computational engine 12, based on the execution of the power saving algorithm 22, produces a system clock control signal 44. The system clock control signal 44 is determined based on the particular application or applications being performed by the computational engine 12 and the processing requirements associated therewith. For example, if the computational engine is performing application 24, and application 24 has a processing requirement of five MIPS (millions of instructions per second), the power savings algorithm 22 would cause the computational engine 12 to set the system clock control signal 44 such that the system clock 42 produces at least a 5Mhz clock. The phase lock loop 16 receives the system clock control signal 44, which is used to address at least one of registers 29, 37 or 39. Based on the addressed value in the corresponding register, the divider 28, 36 or 38 is set to the corresponding value. Once this is done, the phase lock loop 16 performs in a conventional manner.

In addition to generating the system clock control signal 44, the computational engine 12 also produces a power supply control signal 64. The computational engine 12 provides the power supply control signal 64 to the on-chip power supply 20. The on-chip

power supply 20 includes a regulation module 46, an N-channel transistor 48, a P-channel transistor 50, a programmable divider network 54 and 56 and a capacitor 52.

Based on the power supply control signal 64, the on-chip power supply 20 sets the programmable divider such that the regulation module produces supply 58 at a desired value. For example, once the system clock 42 has been set, the supply 58 may be varied such that the processing of the application 24 within the computational engine 12 is optimized. This concept will be discussed in greater detail with reference to Figure 3, 4, 6 and 7. For a more detailed discussion on the on-chip power supply 20, refer to co-pending Patent Application having a Docket Number of SIG000010, entitled METHOD AND APPARATUS FOR REGULATING A DC OUTPUT VOLTAGE, having a Serial Number of 09/551,123, and a filing date of April 18, 2000.

Figure 2 illustrates a schematic block diagram of an alternate integrated circuit in accordance with the present invention. The integrated circuit 70 includes the memory 14, the computational engine 12, the phase lock loop 16, the on-chip power supply 20 and a training module 72. The integrated circuit 70 is coupled to an external inductor 60 and an external power source 62. As with the integrated circuit 10 of Figure 1, the memory 14 may also include an off-chip portion for storing multiple applications. In this configuration, the training module 72 establishes the rate at which the system clock 42 will be generated and the values of supply 58 and supply 84.

In this embodiment, the on-chip power supply 20 produces two supplies 58 and 84. The regulation module 46 regulates the supplies 58 and 84 by controlling switching of transistors 48, 50 and 76. A 2nd feedback divider 80 and 82 is provided to sample the supply 84, which is produced across capacitor 78.

The training module 72, based on the application to be executed by the computational engine 12 establishes the rate of the system clock 42 and the values of supplies 58 and 84. To do this, the training module 72 determines the processing transfer characteristics of the computational engine. The processing transfer characteristics of the

computational engine include propagation delays through logic circuits, slew rates of transistors within memory, logic circuits, read/write processing speed, et cetera, and any other characteristic of a logic circuit, digital signal processor, microprocessor, et cetera that corresponds to the speed at which digital information may be processed. Figures 3 and 4 illustrate embodiments performed by the training module 72.

Figure 3 illustrates a schematic block diagram of a multiply accumulator 90 that may be contained within computational engine 12 or within the training module 72, which may be used in a particular application. The multiply accumulator 90 includes a multiplier 92, an adder 94, and an accumulation register 96. In operation, a data input 98 is multiplied with a coefficient 102 to produce a resultant. The resultant is summed via adder 94 with previous summed data 100 to produce a new accumulated value that is stored in accumulation register 96. The processing transfer characteristics of the computational engine will map the processing characteristics of the multiply accumulator 90 and will vary depending on the voltage set for the supply. What voltage to set for the supply is determined by experimentation once the processing requirements of an application are determined (i.e. the MIPS required). For example, if the MIPS required is one, then the clock rate is set to 1 MHz, thus yielding a period of 1 microsecond. The supply voltage is set for a predetermined low value, then a multiply accumulate function is processed in a known number of clock cycles. If the accumulated value is as expected, the supply voltage is set to this predetermined low level. If, on the other hand, the accumulated value is not as expected, the supply voltage is increased at an incremental rate of 10 mVolts to 500 mVolts, and the accumulation process is repeated. Once the accumulated value is as expected, i.e., the correct value has been accumulated, the supply is set to this value.

Figure 4 illustrates a graphical representation of determining the processing transfer characteristics and processing requirements associated with processing at least a portion of an application. The application may include the MIPS required for processing the entire application or it may include separate indications for each sub routine contained therein. Alternatively, a default processing requirement may be selected for

certain applications or all applications. As one of average skill in the art will appreciate, there is a multitude of ways in which the processing requirements associated with an application may be derived.

Based on the most difficult processing requirements of an application, the system clock 42 is set to provide a clock that at least meets the processing requirements. For example, if the processing requirement is 6 MIPS, the system clock will be set at a rate of at least 6Mhz. Having done this, the supply 58 or 84, which may be a regulated voltage supply or a regulated current output, is varied to change the processing speed of the circuitry within the computational engine. As shown in Figure 4, the processing speed of data input 98 may vary 110 due to changes in the supply. As is known, the lower the supply, the longer it takes digital circuitry to reach a final logic 0 or logic 1 state. As such, as the supply is increased, the processing speed of inputting data and outputting data 100 is increased. The cross hatched areas of data in 98 and data out 100 correspond to the variations in processing speeds of inputting data and outputting data of the multiply accumulator 90 of Figure 3 as the supply voltage is varied. The lower the supply voltage is, the longer it takes to input data and output data. If the supply is too low, the data output 100 will not occur before the next given number of cycles of the system clock 42, i.e., operational period of the system. When this occurs, the supply is set too low. Accordingly, the supply is increased, as shown by the arrow associated with the vertical dash line until the processing speed of the multiply accumulator 90 produces a digital output 100 that occurs just within the period of the system clock 42. A further increase in supply provides no added processing benefit; it only increases the power consumption. Thus, the supply is set so that the data output 100 just completes prior to the beginning of the next clock cycle of system clock 42.

As an alternate processing of the training module 72, a read function may be processed by the computational engine in conjunction with the transfer module. On the command bus 102, a read instruction 106 is placed. Again, based on the supply voltage, the speed of placing of an instruction on the command bus varies. The higher the voltage, the more quickly the command is placed on the bus. Once the read instruction

106 has been interpreted by memory, a data word 108 is placed on a data bus 104. Similarly, the speed at which data may be placed on the data bus 104 is dependent on the supply voltage. The lower the supply voltage, the longer it takes. Thus, to optimize power consumption, the supply voltage is increased until the point where the data word 108 is placed on the data bus 104 is just within the end of the current clock cycle 42 or the clock cycle when the data is expected. By controlling the system clock and supply voltage in this manner, power consumption of an integrated circuit may be optimized based on the corresponding application being performed and the processing characteristics of the computational engine. As one of average skill in the art will appreciate, the computational engine may process multiple applications at a given time. Accordingly, the clock rate would be set such that the speed needed for processing multiple applications is met.

Figure 5 illustrates a schematic block diagram of a power efficient integrated circuit that includes a power controlling apparatus 120 operably coupled to an external inductor 60 and an external power source 62. The power controlling apparatus 120 includes a processing module 122 and a memory 124. The power controlling apparatus 120 is also operably coupled to receive a reference clock 40.

The processing module 122 may be a single processing device or a plurality of processing devices. The processing device may be a microprocessor, microcontroller, microcomputer, digital signal processor, logic circuit, state machine, and/or any device that manipulates signals (analog or digital) based on operational instructions. The memory 124 may be a single memory device or a plurality of memory devices. Such a memory device may be a read only memory, floppy disk memory, random access memory, external memory, and/or any device that stores digital information. Note that when the processing module 122 implements one or more of its functions via a state machine or logic circuit, the memory storing the corresponding operational instructions is embedded within the circuitry comprised in the state machine or logic circuit. The operational instructions stored in memory 124 and executed by processing module 122 are further illustrated in Figures 6 and 7.

Figure 6 illustrates a logic diagram of a method for controlling power consumption of an integrated circuit. The process begins at Step 130 where a system clock is produced from a reference clock based on a system clock control signal. As is known, a processing module may include functional components to perform a digital, or analog, phase lock loop that is controlled by the system control clock signal. The process then proceeds to Step 132 where at least one supply is regulated from a power source and an inductor based on a power supply control signal or from a linear regulator.

The process then proceeds to Step 134 where the system clock control signal and the power supply control signal are produced based on a processing transfer characteristic of a computational engine and processing requirements associated with processing at least a portion of an application. Note that the computational engine may be included within the processing module 122 or a separate device that includes logic circuitry, a state machine, digital signal processor, digital circuitry, analog circuitry, and/or a combination thereof.

The processing transfer characteristics of the computational engine may be further determined as described in Step 136. At Step 136 the processing transfer characteristic and the processing requirements are determined based on a known executional requirements of a given function. The known executional requirement includes at least one of a specification of millions of instructions per second (MIPS) required to process at least a portion of an application, timing requirement between dependent operations (e.g. the timing requirement between inputting a request to RAM and receive data back), and speed of execution (e.g. slew rate of transistors within the circuitry comprising the computational engine).

Steps 136-A and 136-B further illustrate the determination of the transfer characteristics and the processing requirements. At Step 136-a a 1st system clock control signal is determined based on the MIPS required to complete the given function such that the system clock is set to a minimum frequency to meet the MIPS required. For example,

if the processing requirements of the known function is 6 MIPS, the system clock is set to a value of 6Mhz or slightly greater than 6Mhz. At Step 136-B, the power supply control signal is incremented causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result. This was illustrated and discussed with reference to Figure 4 when processing the multiplied accumulate function and/or the read function.

Figure 7 illustrates various processing steps that further describe corresponding steps of Figure 6. Step 132-A further describes the regulation of at least one supply by adjusting a programmable divider circuit of the on-chip power supply based on the control signal. Step 132-B further includes regulating the at least one supply by regulating multiple supplies from the system clock and multiple power supply control signals, where each of the multiple power supply control signals corresponds to an unique one of the multiple supplies. This was illustrated in Figure 2 where power supply control signal 64 regulates supply 58 and power supply control signal 74 regulates supply 84.

The production of the system clock may be further described with reference to Steps 140 and 142. At Step 140, a register is accessed based on the system clock control signal to retrieve a selected divider setting. The process then proceeds to Step 142 where a divider setting of a divider in the phase lock loop is adjusted to produce the system clock in accordance with the selected divider setting.

The preceding discussion has presented a method and apparatus for controlling power consumption within an integrated circuit. By adjusting the system clock and/or the supply based on application being executed by the integrated circuit, power consumption may be optimized. As one of average skill in the art will appreciate, other embodiments may be derived from the teachings of the present invention without deviating from the scope of the claims. For example, a buck converter may be instead of a boost converter, or a combination of a buck and boost converter may be used.

CLAIMS

What is claimed is:

1. A power efficient integrated circuit comprising:

phase lock loop operably coupled to receive a reference clock and to produce therefrom a system clock based on a system clock control signal;

on-chip power supply control module operably coupled to regulate at least one supply from a power source and an inductance based on a power supply control signal;

memory operably coupled to store at least one application; and

computational engine operably coupled to produce the system clock control signal and the power supply control signal based on a processing transfer characteristic of the computation engine and processing requirements associated with processing at least a portion of the at least one application.

2. The power efficient integrated circuit of claim 1, wherein each of the at least one application comprises the processing requirements for at least one of: each sub-routine contained in the application and the application.

3. The power efficient integrated circuit of claim 1, wherein the computational engine further comprises:

training module operably coupled to determine the processing transfer characteristic and the processing requirements based on a known executional requirements of a given function, wherein the known executional requirements includes at least one of: millions of instructions per second (MIPS), timing requirement between dependent operations, and speed of execution.

4. The power efficient integrated circuit of claim 3, wherein the given function further comprises at least one of: reading from memory, executing a test multiply-accumulate function, and propagating data through combinational logic circuit.

5. The power efficient integrated circuit of claim 4, wherein the training module further comprises:

system clock determining module operably coupled to determine a first system clock control signal based on MIPS required to complete the given function such that the system clock is set to a minimum frequency to met the MIPS required; and

power supply determining module operably coupled to increment the power supply control signal causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result.

6. The power efficient integrated circuit of claim 1, wherein the phase lock loop further comprises:

at least one divider module; and

a register operably coupled to the at least one divider module, wherein the register stores various divider values that are selected based on the system clock control signal.

7. The power efficient integrated circuit of claim 1, wherein the on-chip power supply further comprises a programmable divider circuit that is programmed based on the power supply control signal.

8. The power efficient integrated circuit of claim 1, wherein the at least one supply further comprises multiple supplies that are produced from the system clock and multiple

power supply control signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies.

9. A method for controlling power consumption of an integrated circuit, the method comprises the steps of:

producing a system clock from a reference clock based on a system clock control signal;

regulating at least one supply from at least one of: a linear regulator and a power source and an inductance based on a power supply control signal; and

producing the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computation engine and processing requirements associated with processing at least a portion of an application by the computation engine.

10. The method of claim 9 further comprises retrieving the processing requirements from the application.

11. The method of claim 9 further comprises:

determining the processing transfer characteristic and the processing requirements based on a known executional requirements of a given function, wherein the known executional requirements includes at least one of: millions of instructions per second (MIPS), timing relationship between dependent operations, and speed of execution.

12. The method of claim 11 further comprises:

determining a first system clock control signal based on MIPS required to complete the given function such that the system clock is set to a minimum frequency to met the MIPS required; and

incrementing the power supply control signal causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result.

13. The method of claim 9, wherein the producing the system clock from a reference clock based on a system clock control signal further comprises:

accessing a register based on the system clock control signal to retrieve a selected divider setting; and

adjusting a divider setting of a dividing in a phase lock loop that produces the system clock based on the selected divider setting.

14. The method of claim 9, wherein the regulating at least one supply further comprises adjusting a programmable divider circuit of an on-chip power converter based on the power supply control signal.

15. The method of claim 9, wherein the regulating the at least one supply further comprises regulating multiple supplies from the system clock and multiple power supply control signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies.

16. An apparatus for controlling power consumption of an integrated circuit, the apparatus comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

produce a system clock from a reference clock based on a system clock control signal;

regulate at least one supply from at least one of: a linear regulator and a power source and an inductance based on a power supply control signal; and

produce the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computation engine and processing requirements associated with processing at least a portion of an application by the computation engine.

17. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to retrieve the processing requirements from the application.

18. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to:

determine the processing transfer characteristic and the processing requirements based on a known executional requirements of a given function, wherein the known executional requirements includes at least one of: millions of instructions per second (MIPS), timing relationship between dependent operations, and speed of execution.

19. The apparatus of claim 18, wherein the memory further comprises operational instructions that cause the processing module to:

determine a first system clock control signal based on MIPS required to complete the given function such that the system clock is set to a minimum frequency to met the MIPS required; and

increment the power supply control signal causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result.

20. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to produce the system clock from a reference clock based on a system clock control signal by:

accessing a register based on the system clock control signal to retrieve a selected divider setting; and

adjusting a divider setting of a dividing in a phase lock loop that produces the system clock based on the selected divider setting.

21. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to regulate at least one supply by adjusting a programmable divider circuit of an on-chip power converter based on the power supply control signal.

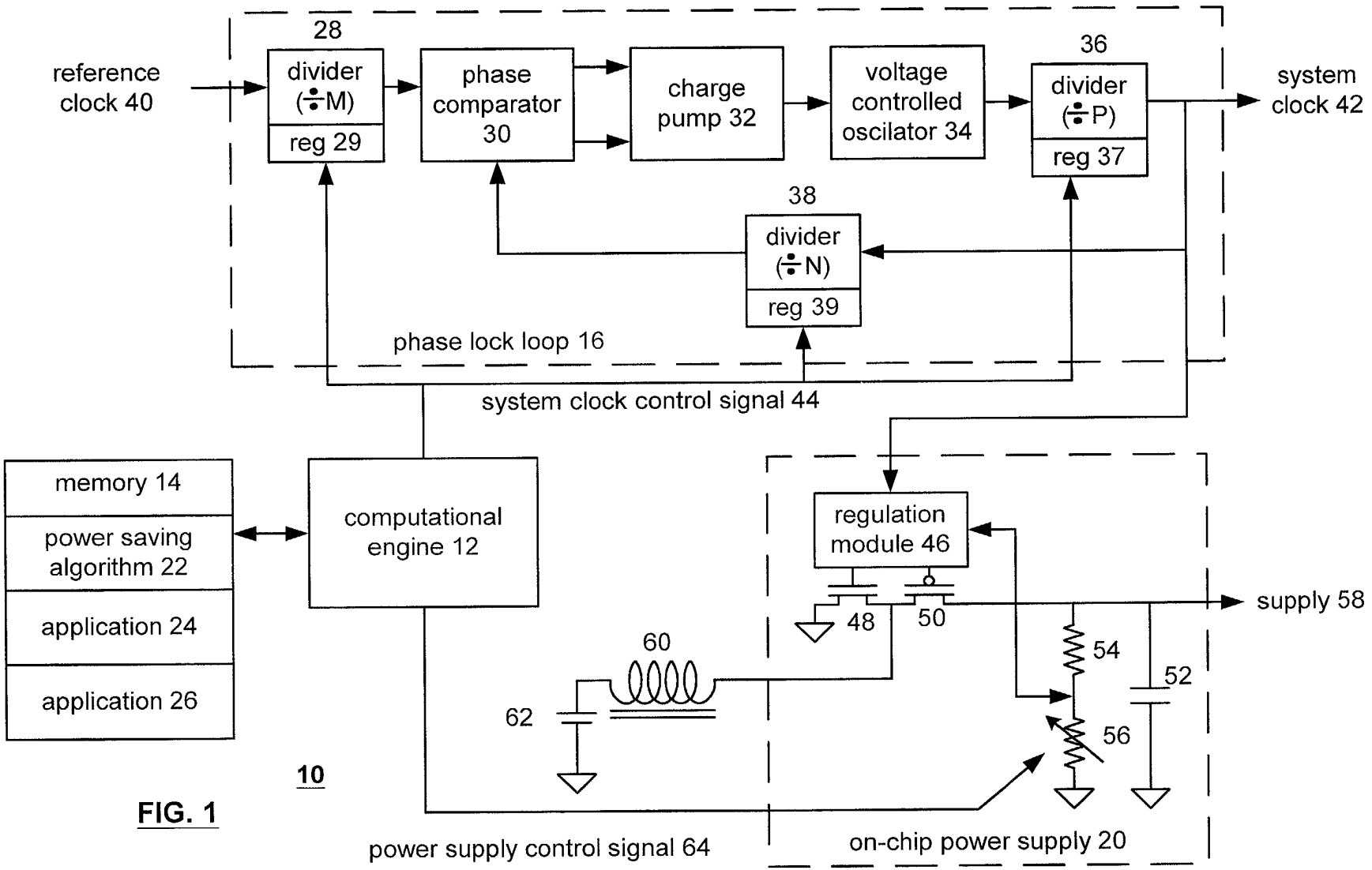
22. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to regulate the at least one supply by regulating multiple supplies from the system clock and multiple power supply control

signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies.

A METHOD AND APPARATUS FOR CONTROLLING POWER CONSUMPTION OF AN INTEGRATED CIRCUIT

ABSTRACT OF THE DISCLOSURE

A method and apparatus for controlling power consumption of an integrated circuit include processing that begins by producing a system clock from a reference clock based on a system clock control signal. The reference clock may be generated from an external crystal oscillator circuit operable to produce a reference clock at a desired frequency. The processing continues by regulating at least one supply from a power source and an inductor based on a power supply control signal. The processing continues by producing the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computational engine and processing requirements associated with processing at least a portion of an application by the computational engine.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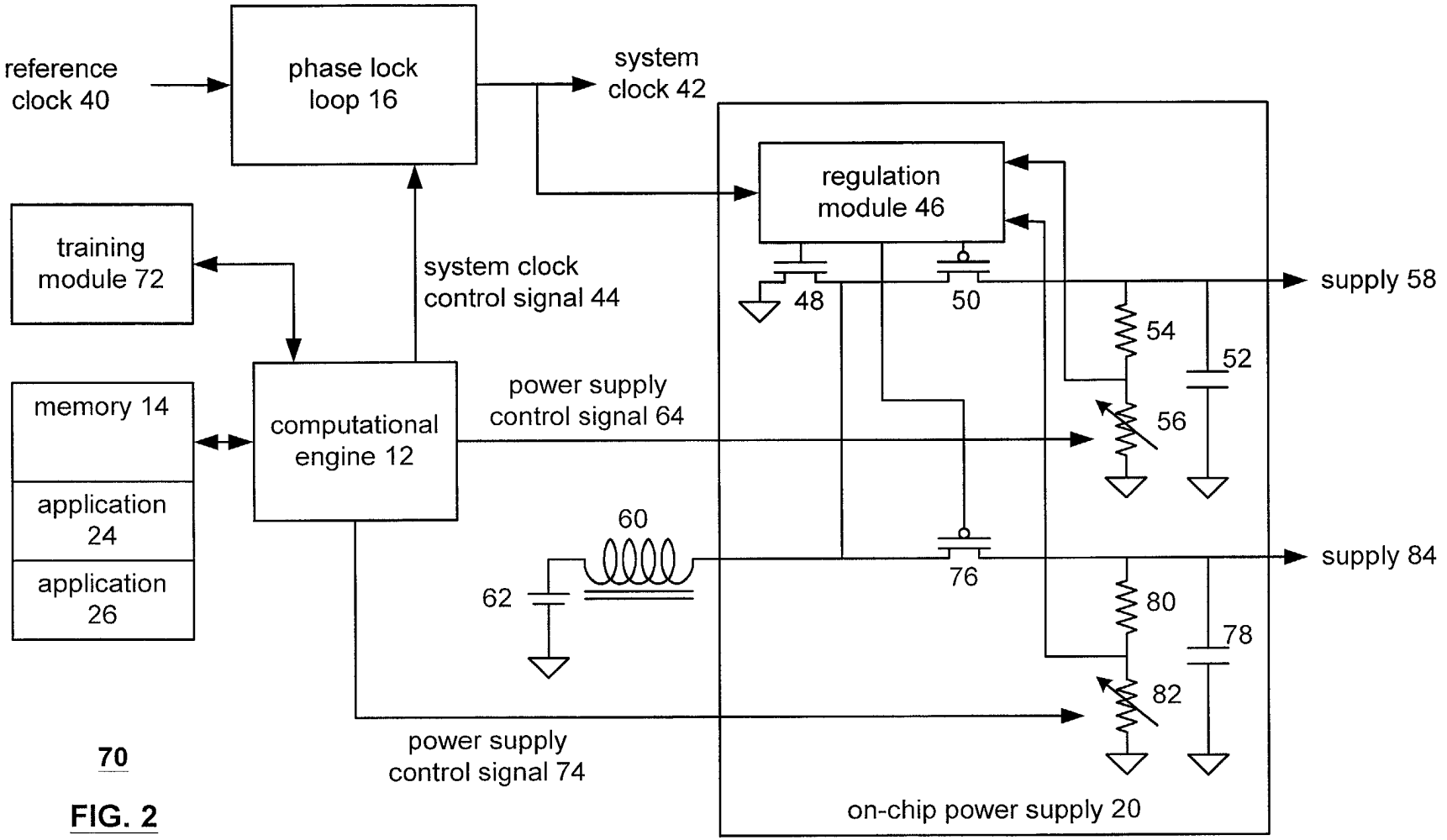
reference clock 40
divider (÷M)
reg 29
phase comparator 30
charge pump 32
voltage controlled oscilator 34
36
divider (÷P)
reg 37
system clock 42
38
divider (÷N)
reg 39
phase lock loop 16
system clock control signal 44
memory 14
power saving algorithm 22
application 24
application 26
computational engine 12
regulation module 46
supply 58
48
50
60
62
54
52
56
10
power supply control signal 64
on-chip power supply 20

FIG. 1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phase lock loop 16
system clock 42
regulation module 46
training module 72
system clock control signal 44
48
50
supply 58
54
52
memory 14
application 24
application 26
computational engine 12
power supply control signal 64
56
60
62
76
supply 84
80
78
82
power supply control signal 74
on-chip power supply 20
70

FIG. 2

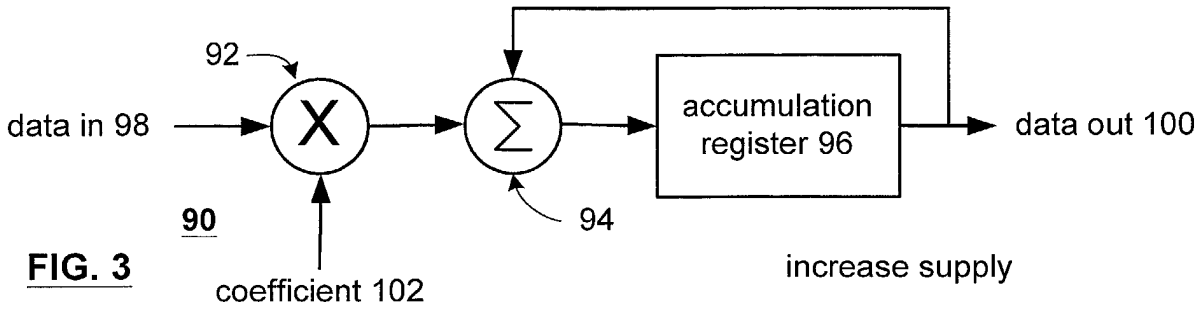

92
data in 98
X
Σ
accumulation register 96
data out 100
90
94
coefficient 102

FIG. 3

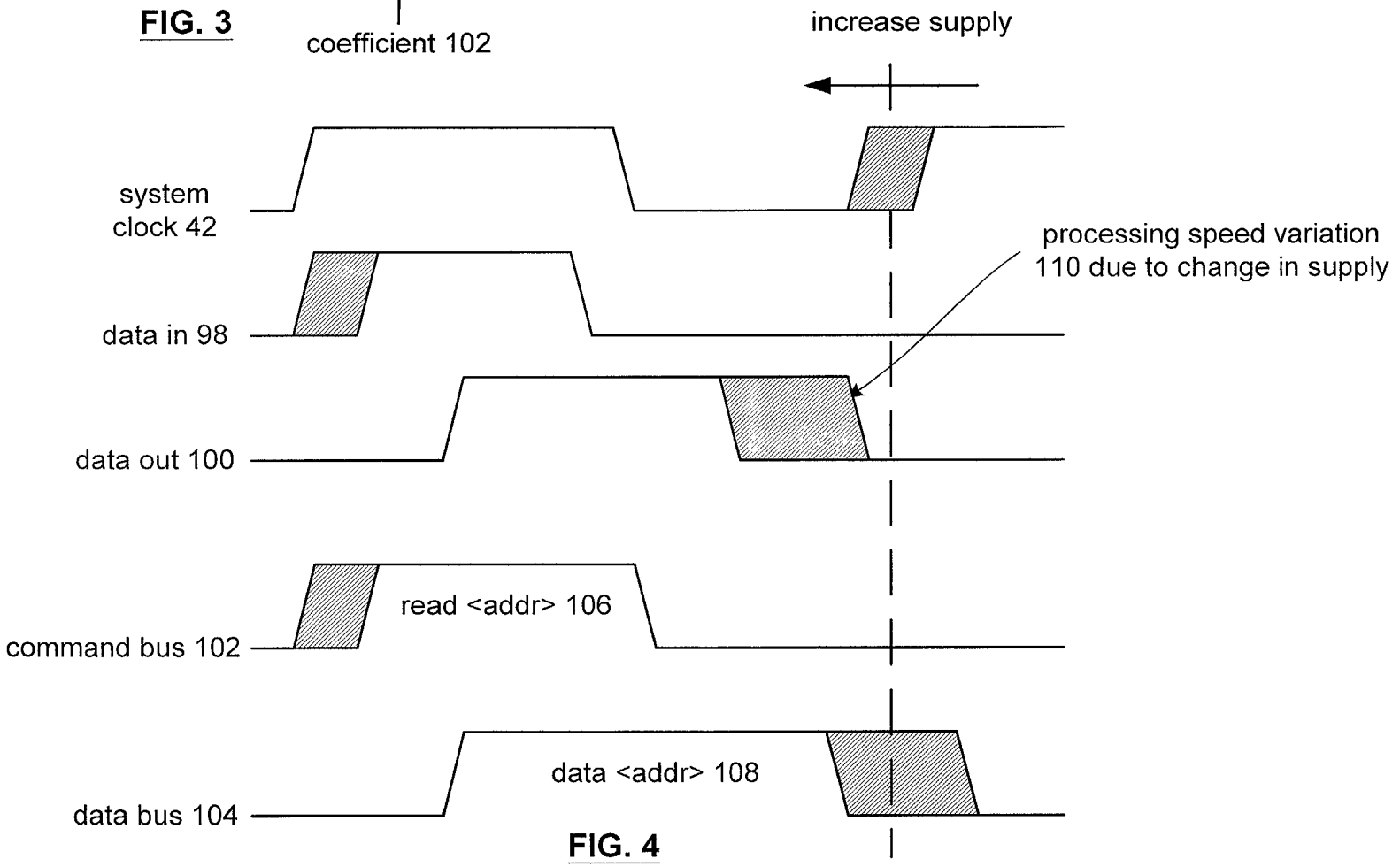

increase supply
system clock 42
processing speed variation 110 due to change in supply
data in 98
data out 100
read <addr> 106
command bus 102
data <addr> 108
data bus 104

FIG. 4

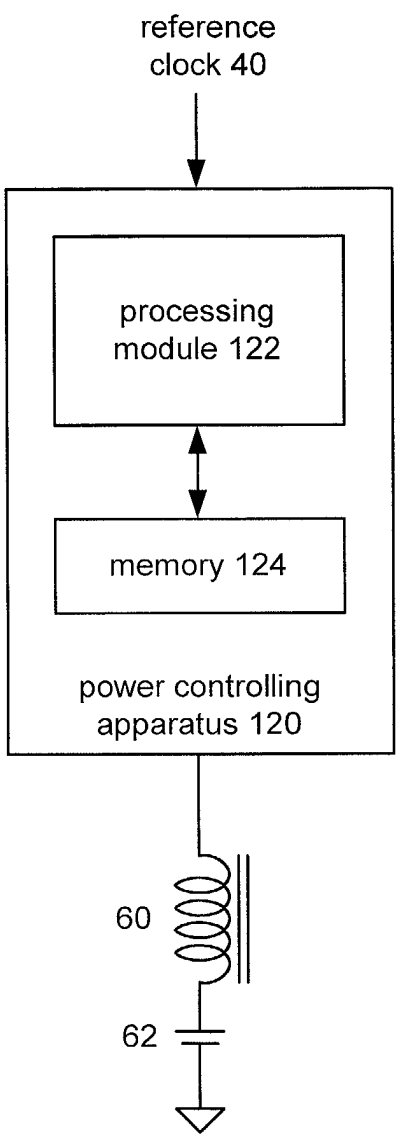


FIG. 5

claim 9

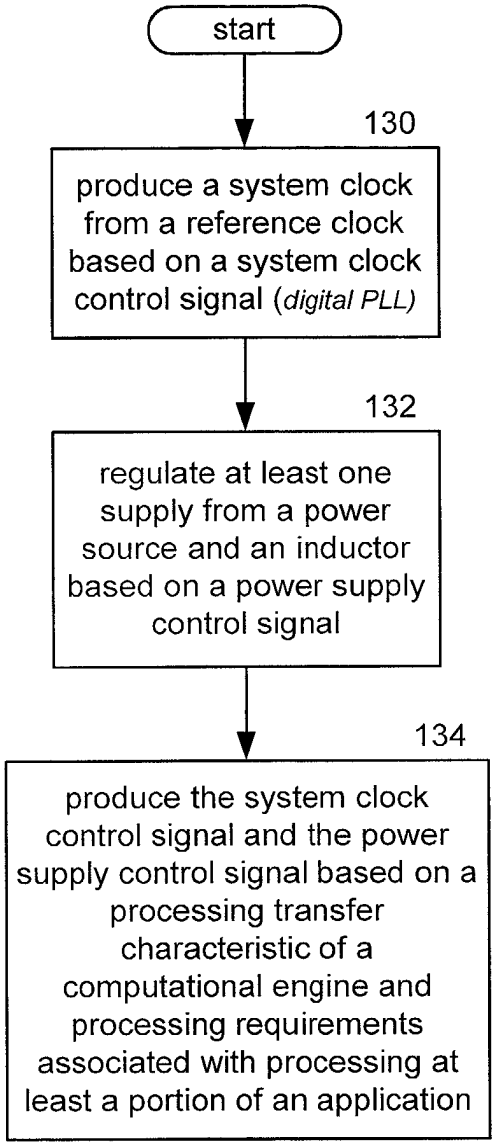
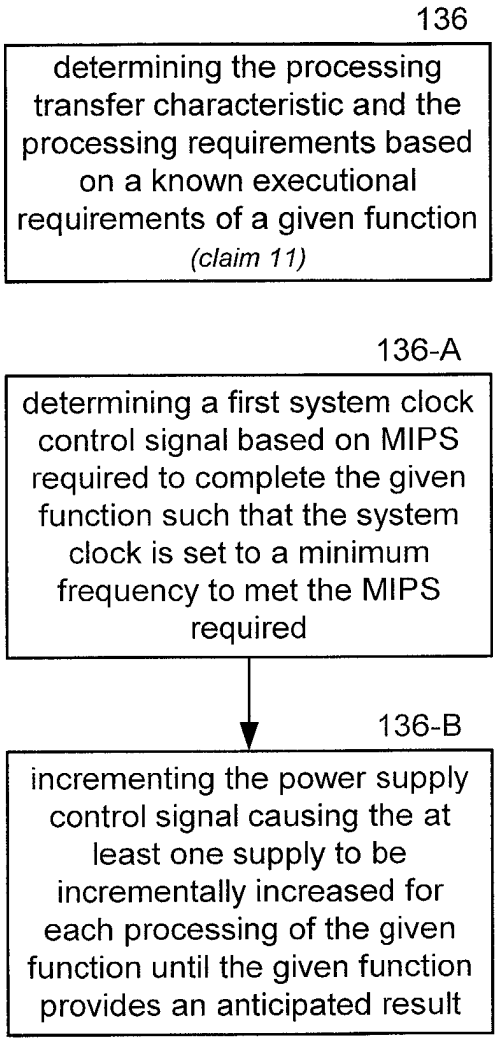


FIG. 6



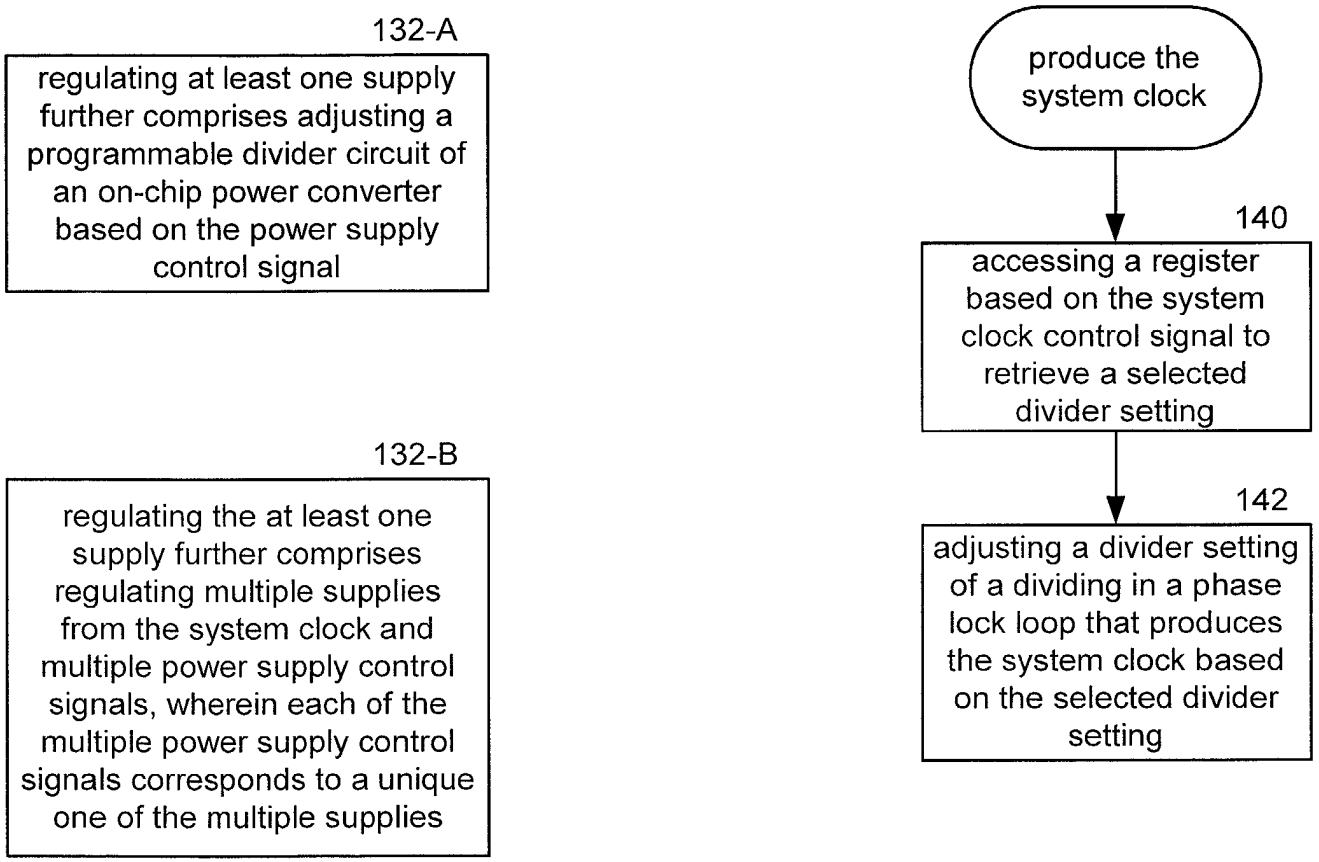

132-A
regulating at least one supply further comprises adjusting a programmable divider circuit of an on-chip power converter based on the power supply control signal
132-B
regulating the at least one supply further comprises regulating multiple supplies from the system clock and multiple power supply control signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies
produce the system clock
140
accessing a register based on the system clock control signal to retrieve a selected divider setting
142
adjusting a divider setting of a dividing in a phase lock loop that produces the system clock based on the selected divider setting

FIG. 7

PATENT APPLICATION
Docket No.: SIG000039

DECLARATION AND POWER OF ATTORNEY
Pursuant to 37 C.F.R 1.63 and 1.67

As a below named inventor, I hereby declare that.
My residence, post office address and citizenship are as stated below next to my name; and
I believe that I an inventor of the subject matter of a patent application entitled:

METHOD AND APPARATUS FOR CONTROLLING POWER CONSUMPTION OF AN INTEGRATED CIRCUIT

The specification for the patent application (check one):

[X] is attached hereto

[ ] was filed on as Application Serial No.
and was amended on (if applicable).

[ ] was filed as PCT International Application No. PCT/ on
and was amended on (if applicable).

[ ] was filed on as Application Serial No.
and was issued a Notice of Allowance on

I hereby state that I have reviewed and understood the contents of the above identified patent application, including the claims as amended by any amendment referred to above or as allowed as indicated above.

I acknowledge the duty to disclose all information known to me to be material to the patentability of this patent application as defined in 37 C.F.R. Section 1.56 If this is a continuation-in-part (CIP) application, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the Office all information known to me to be material to patentability of the application as defined in 37 C.F.R. Section 1.56 which became available between the filing data of the prior application and the national or PCT international filing date of this CIP application.

I hereby claim foreign priority benefits under 35 U.S.C. Sections 119 and 365 of any foreign application(s) for patent(s) or inventor's certificate(s) listed below. I have also identified below any foreign application(s) for patent(s) or inventor's certificate(s) filed by me or my assignee which: disclose the subject matter claimed in this patent application; and have a filing date that is either: (1) before the filing date of the application on which my priority is claimed; or, (2) before the filing date of this application when no priority is claimed:

Prior Foreign Patents
(list number, country, filing date MDY, date laid open, date granted or patented)

I hereby claim the benefit under 35 U S.C Sections 120 and 365 of any United States application(s) listed below and PCT international application(s) listed below:

Prior U.S. or PCT Applications

Application No.	Mo/Day/Yr Filed	Status

I hereby appoint Timothy W. Markison, Registration No. 33,534 of SigmaTel Inc., 2700 Via Fortuna, Sutie 500, Austin, Texas 78746 as my attorney, with full power of substitution and revocation, to prosecute this patent application and to transact all business in the United States Patent and Trademark Office connected therewith, and to file and prosecute any international patent applications filed thereon before any international authorities under the Patent Cooperation Treaty, and I hereby authorize him to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct them in writing to the contrary.

Please address all correspondence and direct all telephone calls to:
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Phone: (512) 381-3732
Fax: (512) 381-4125
Customer No: 000024263

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this patent application or any patent issued thereon.

Inventor(s)

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Mulligan Daniel 500 Bulian Lane Austin Texas 78746	citizen of:	Signature: _____ Date: 11/14/00
	citizen of:	Signature: _____ Date _____
	citizen of:	Signature: _____ Date: _____
	citizen of:	Signature. _____ Date: _____
	citizen of:	Signature: _____ Date. _____